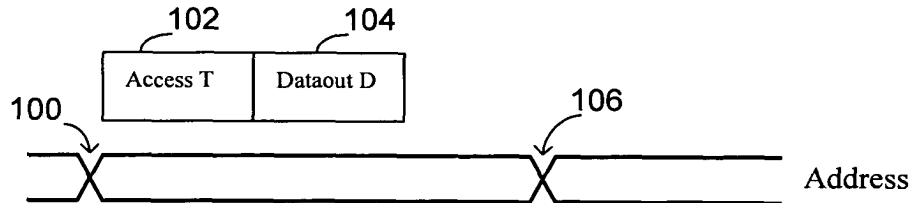
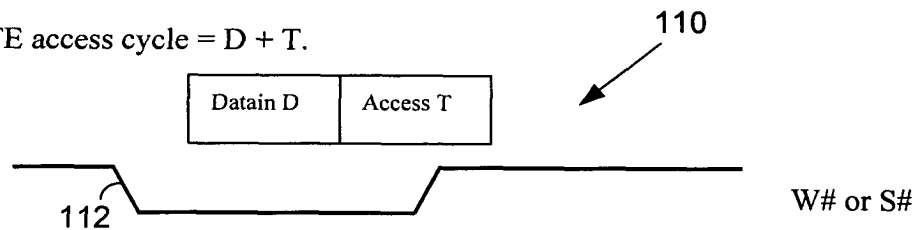


**Prior art: READ and WRITE cycles**

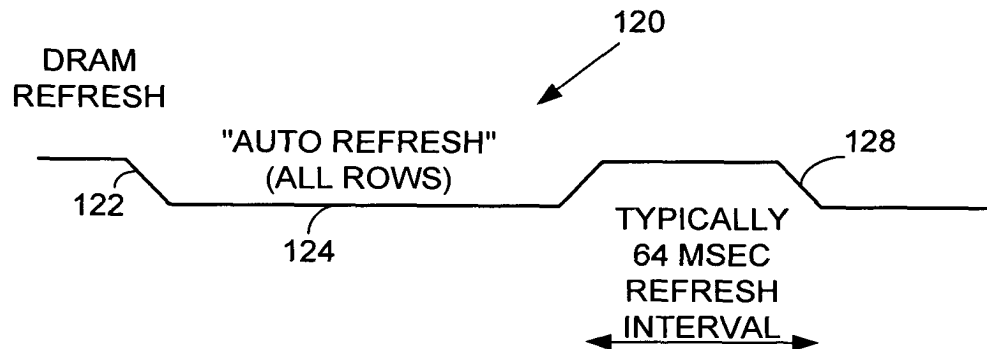
READ access cycle =  $T + D$ .



WRITE access cycle =  $D + T$ .



**FIG. 1A**  
**PRIOR ART**



**FIG. 1B**  
**PRIOR ART**

READ access cycle = T + T + D:

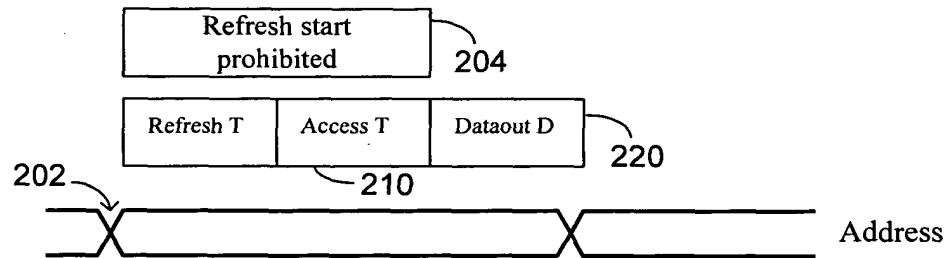


FIG. 2A

WRITE access cycle = D + T + T.

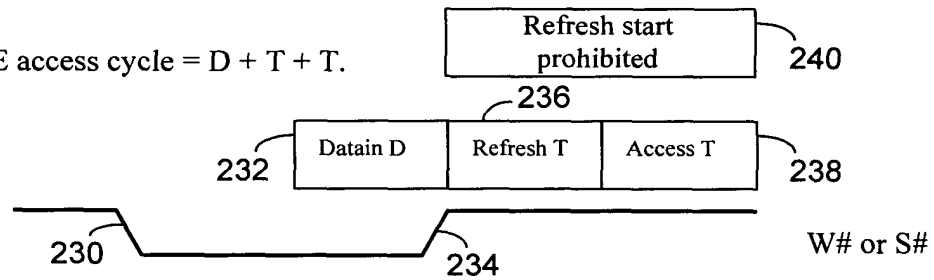


FIG. 2B

Invalid READ, termination during “dataout”

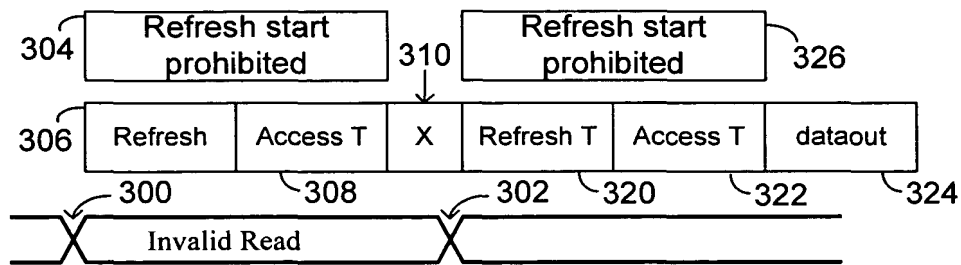


FIG. 3A

Invalid READ, termination during “access”

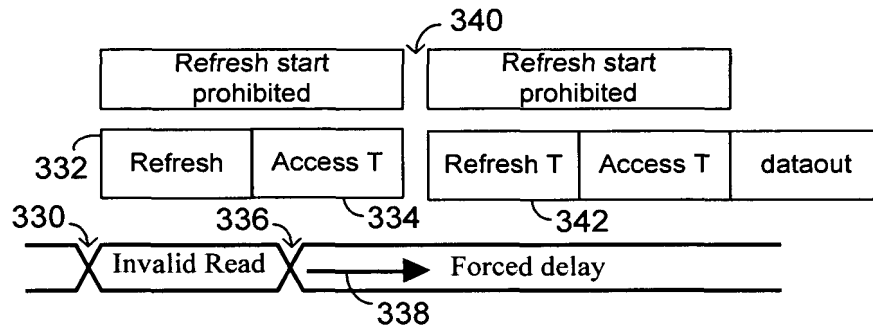


FIG. 3B

Invalid READ, termination during “refresh”

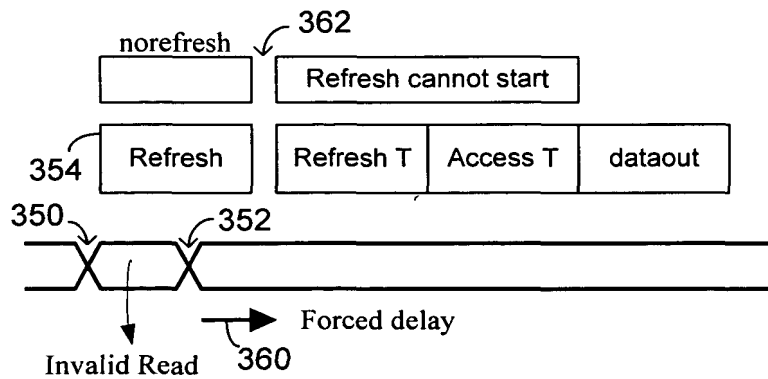
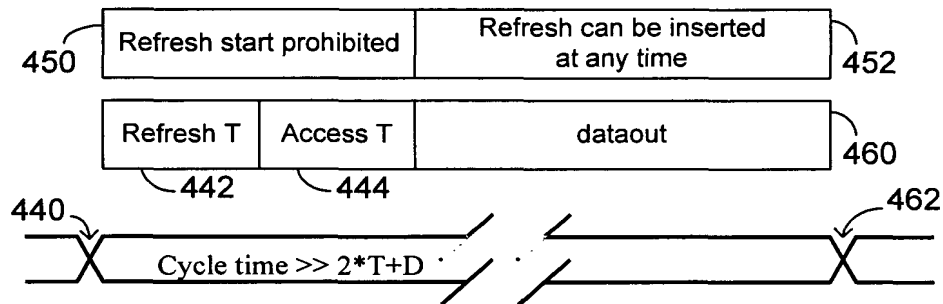


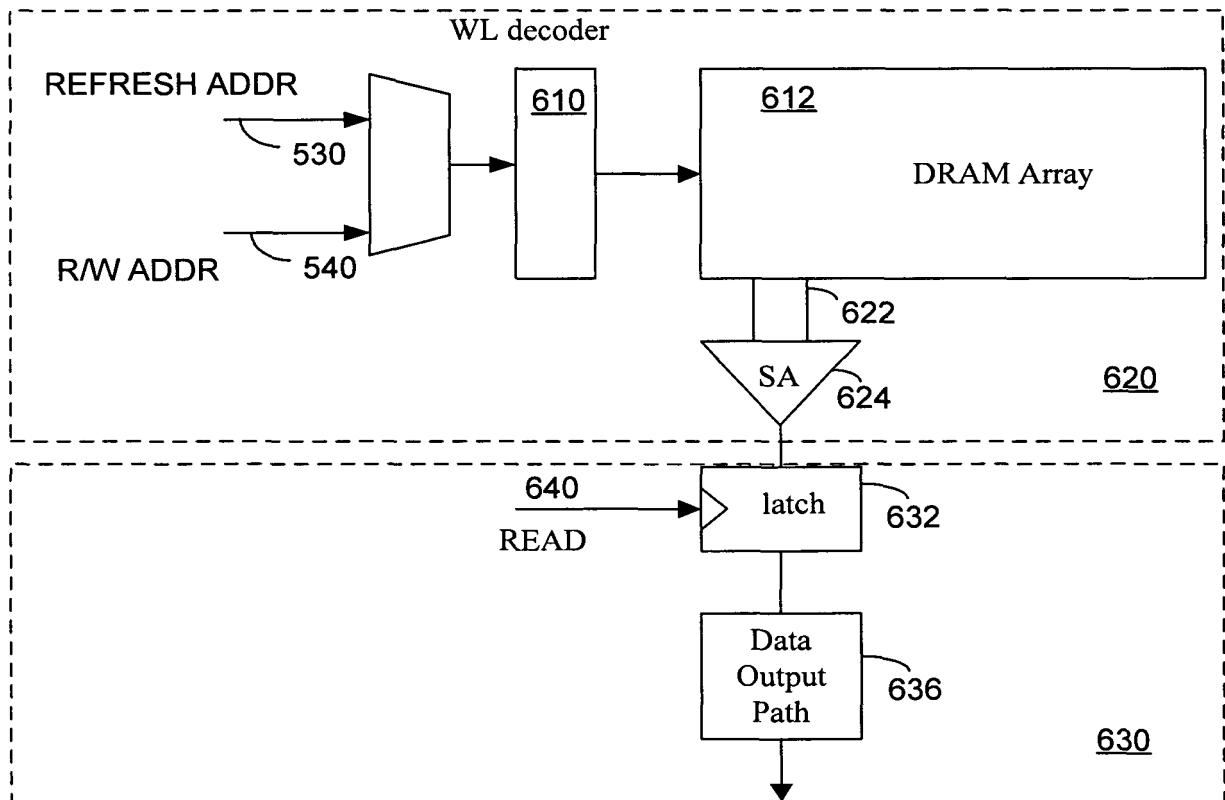
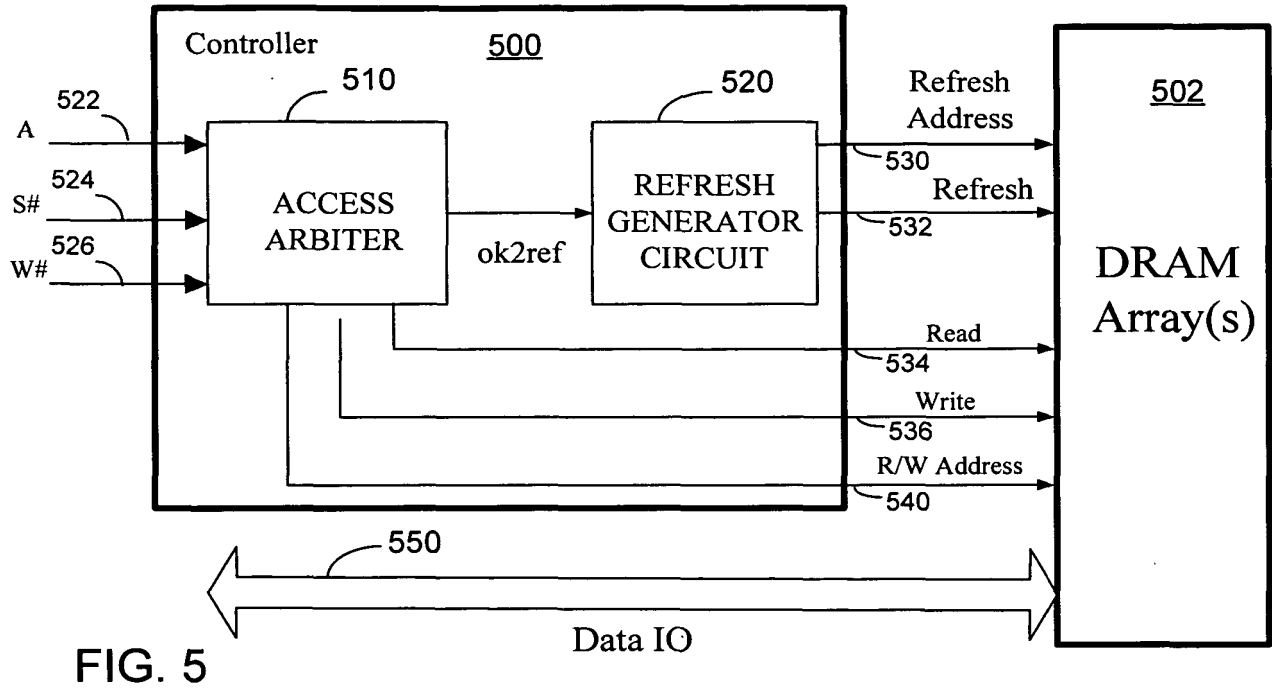
FIG. 3C

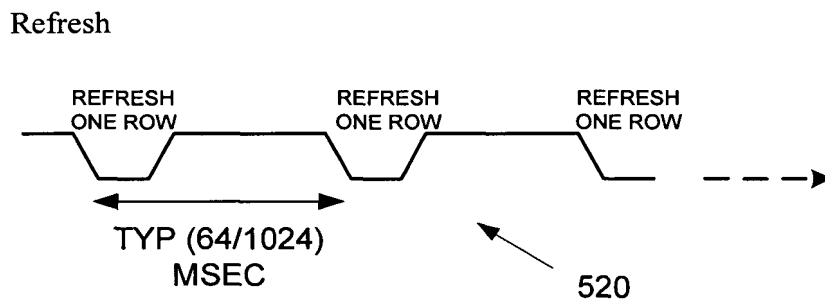
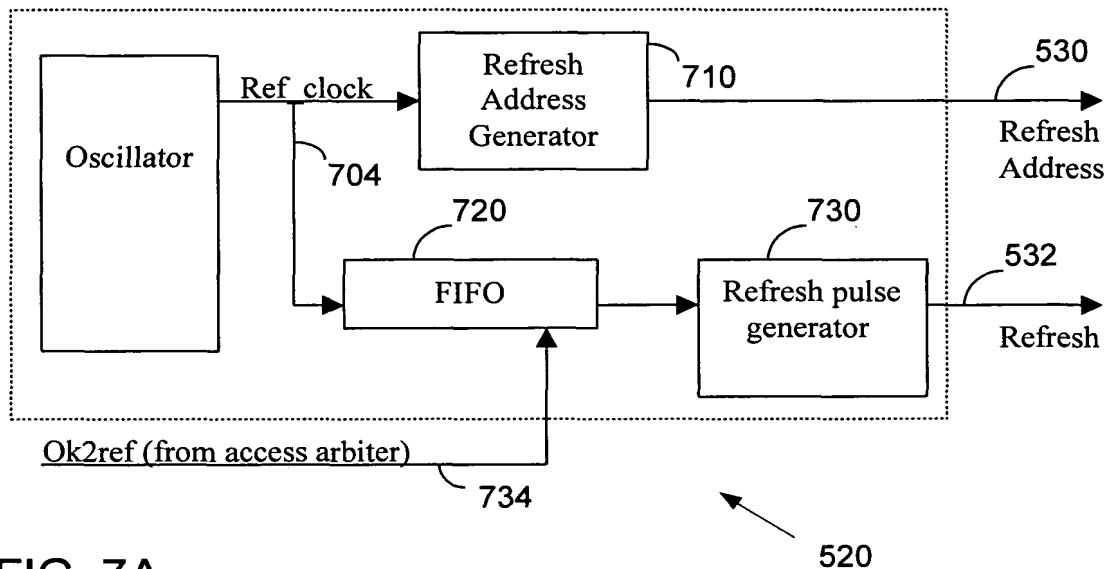
The diagram illustrates the timing of a memory device. It shows two main operation sequences: READ and WRITE. The READ sequence starts with a 'Refresh start prohibited' period (416), followed by a 'delay' (412) before the 'No-op T' (414) period. The WRITE sequence includes 'Datain D' (402), 'Refresh T' (404), and 'Access T' (406). A signal line at the bottom, labeled 'W# or S#', shows a pulse (400) and a subsequent high level (410).

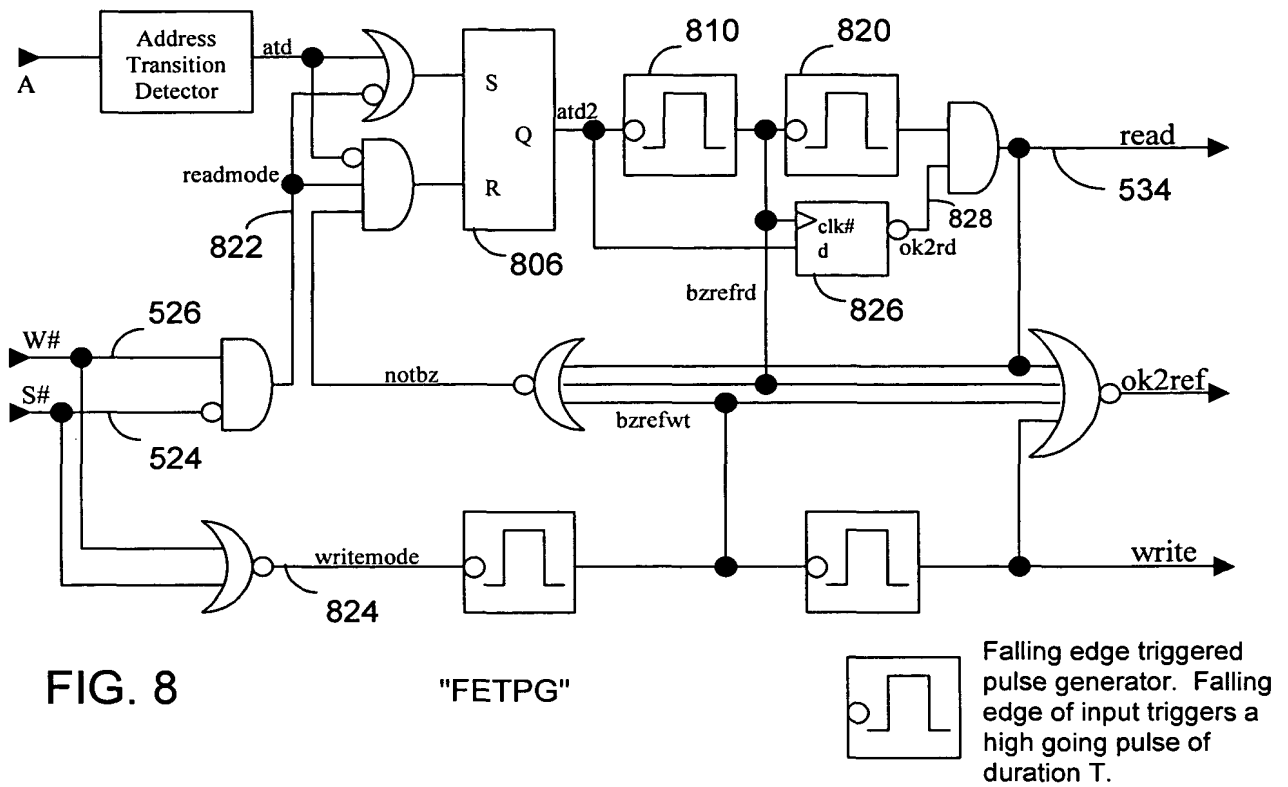
Low frequency READ, refresh operation can be inserted between "access" and "dataout"



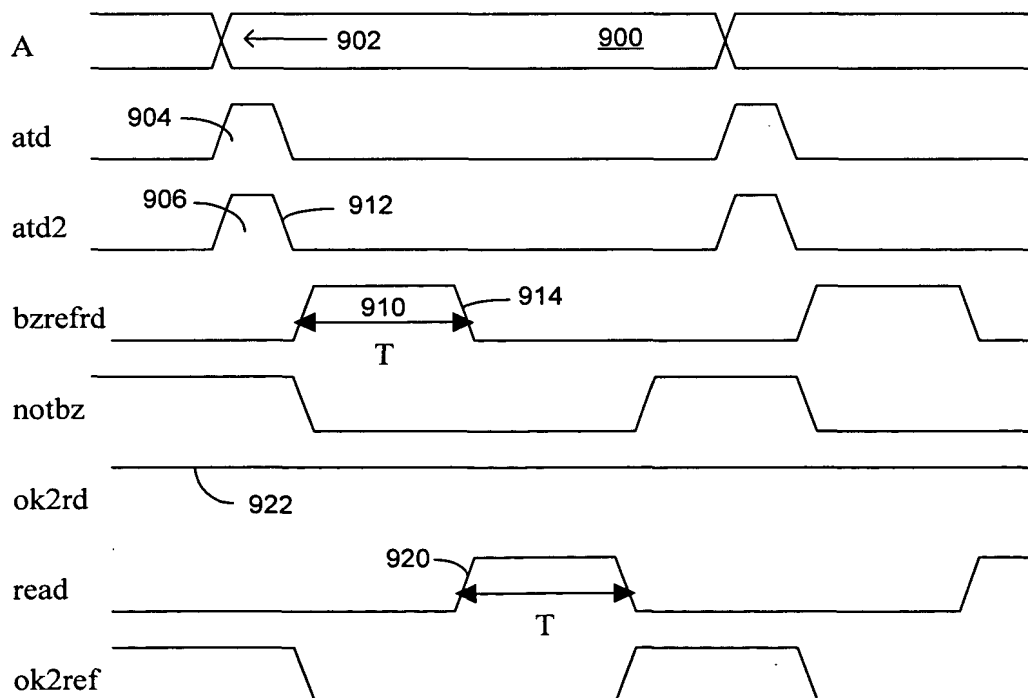
**FIG. 4B**







Timing diagram for a normal read access



**FIG. 9**

Timing diagram for an invalid read  
 operation terminated within T of starting

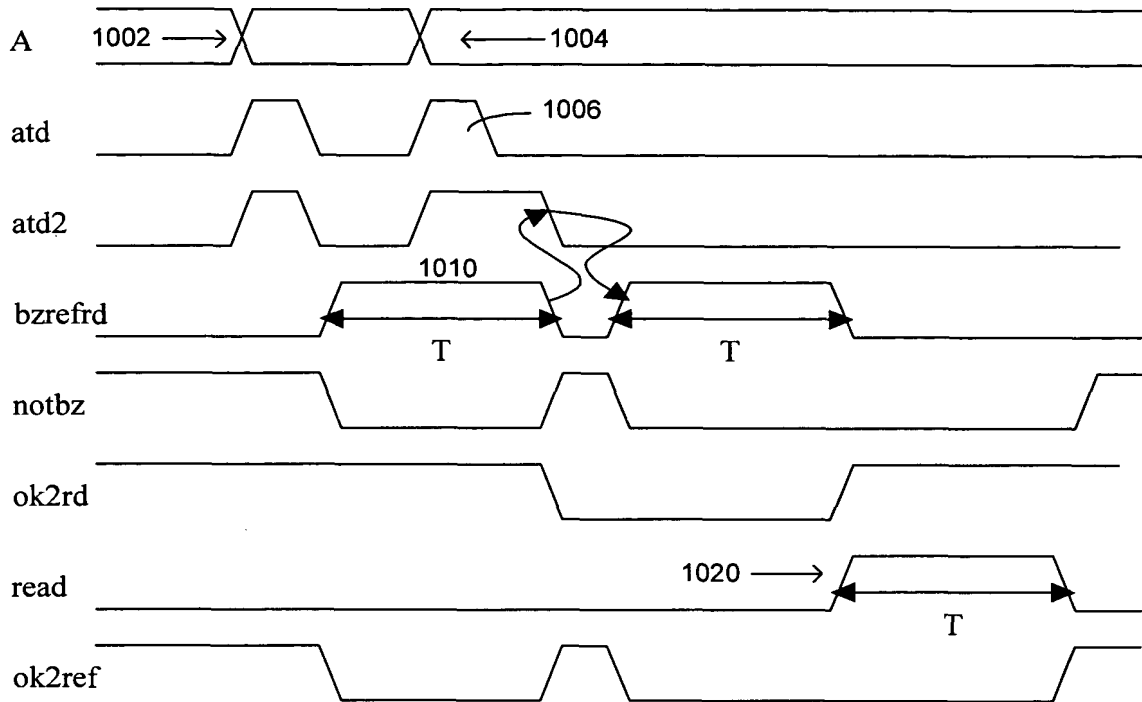


FIG. 10

Timing diagram for an invalid read  
 operation terminated within 2\*T of starting

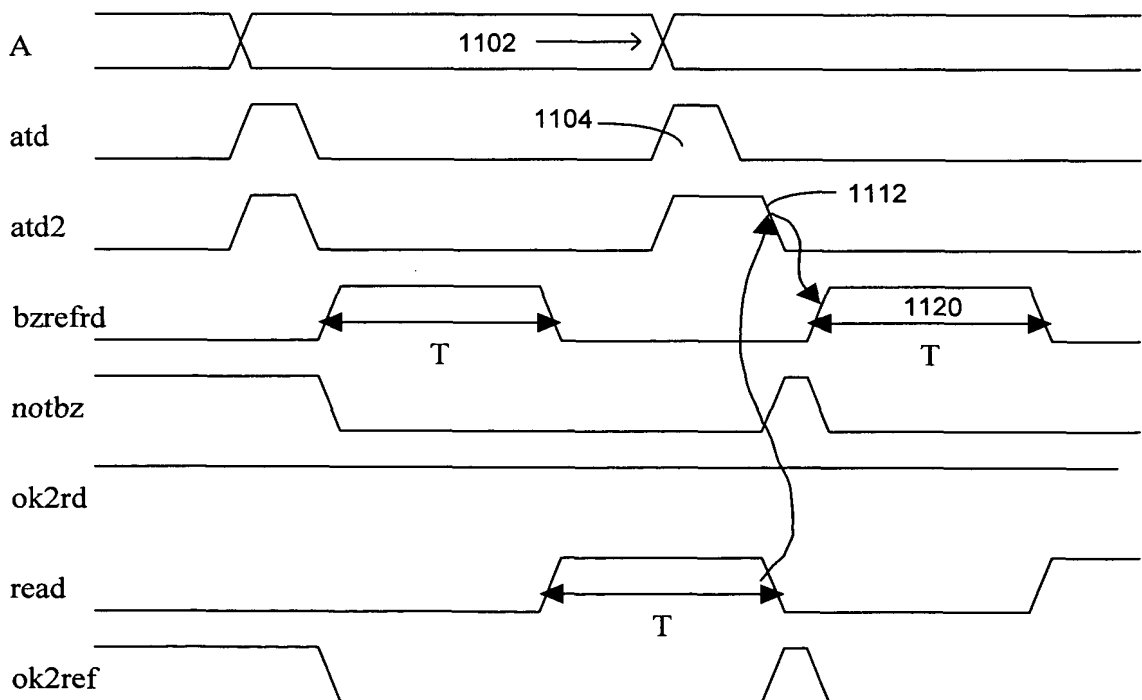


FIG. 11



Timing diagram of a write cycle

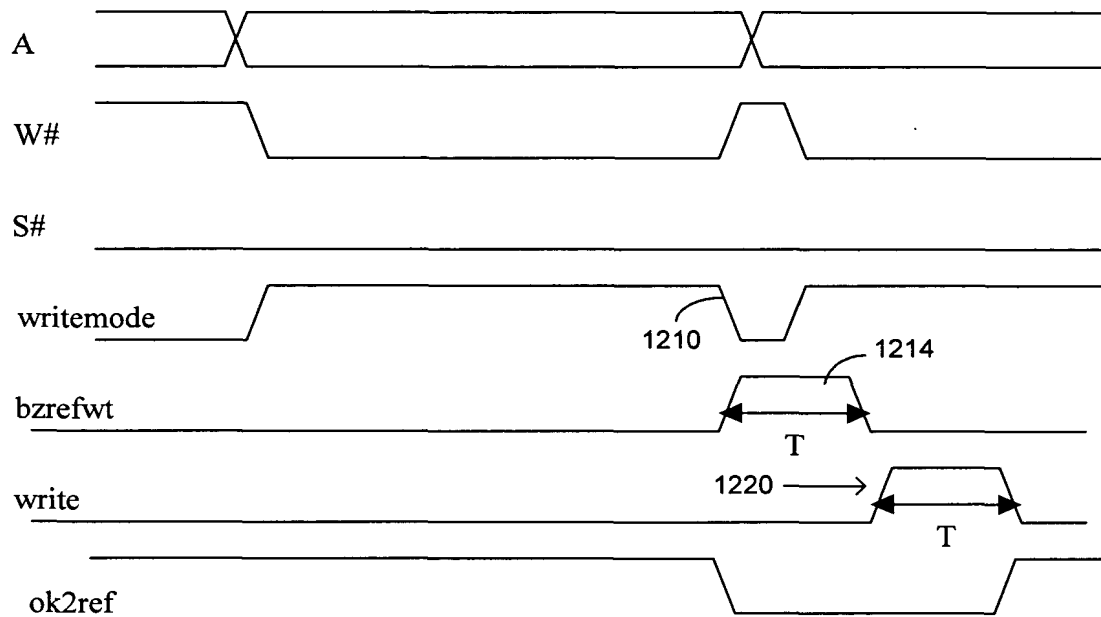


FIG. 12

Timing diagram of a write cycle  
immediately followed by a read

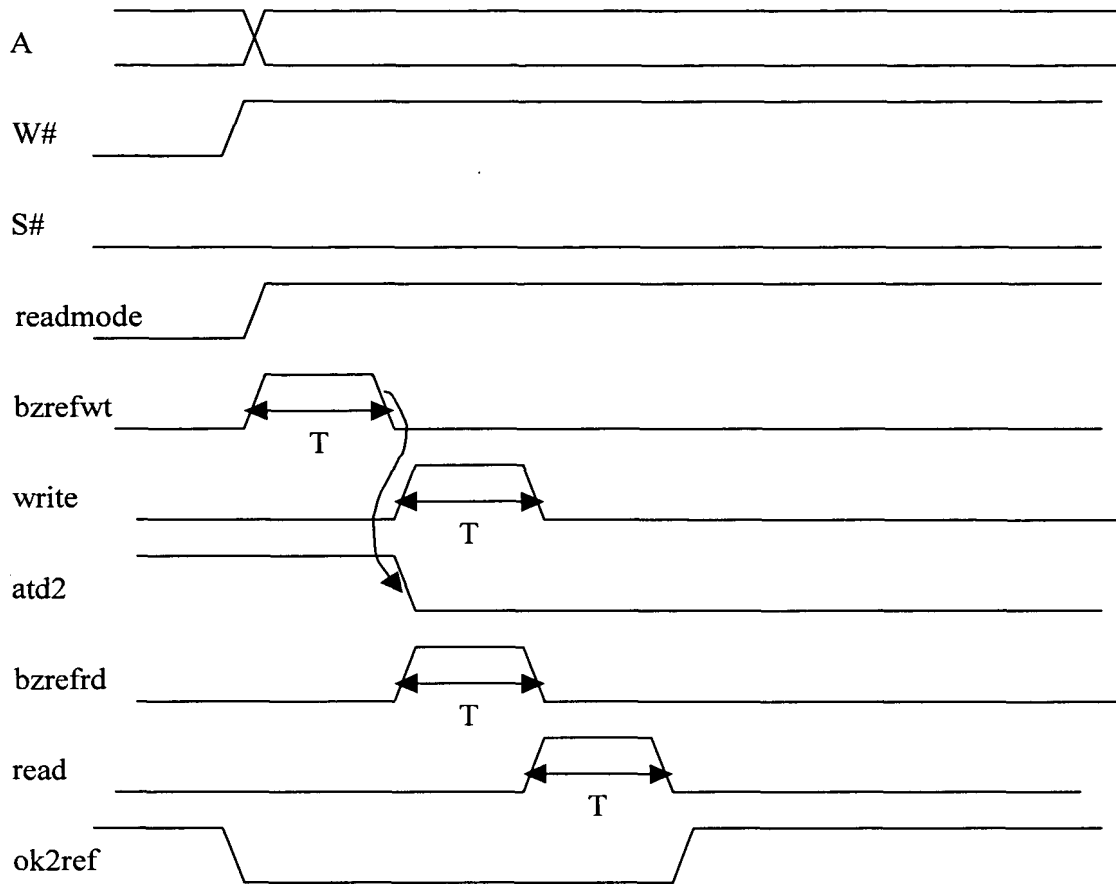


FIG. 13